REMARKS

Claims 1, 2 and 4-11 are pending in this application. The specification has been amended to correct certain typographical errors.

Rejection of Claims 1,2 and 4-11 under 35 USC § 103(a)

Claims 1-2 and 4-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cottle et al. (U.S. Patent No. 6,263,396).

The present claimed invention provides a video apparatus with a digital decoder and process for controlling the video apparatus. A first memory stores video data and a second memory stores on-screen display data. An on-screen display circuit generates an on-screen display graphics signal from the on-screen display data in the second memory. The first memory is adapted to receive on-screen display data that is no longer being displayed from the second memory and transfer the on-screen display data back to the second memory in response to a request for display of data stored in the first memory. Features similar to those discussed above are found in independent claims 1 and 6.

Cottle et al. describe a programmable interrupt controller for a single interrupt architecture processor including a plurality of interrupt sources each operable to generate an interrupt. A dynamically alterable interrupt mask selectively blocks interrupt signals for the interrupt sources. Interrupts permitted by the dynamically alterable interrupt mask are processed by an interrupt handler for the single interrupt architecture processor in order of priority. In addition, processing for a lower priority interrupt is interrupted in order to process a later received higher priority interrupt permitted by the dynamically alterable interrupt mask. Cottle et al., however, neither disclose nor suggest the first memory is adapted "to transfer said on-screen display data back to the second memory in

response to a request for display of data stored in the first memory" as recited in claim 1 of the present invention. Independent claim 6 contains similar features.

The Office Action contends that Cottle et al. disclose SDRAM 312, 32-bit Data RAM 240, TC bus, MPEG Decoder 250, on-screen display (OSD) processor 270, and microprocessor 280 where the SDRAM 312 stores video/audio data as well as OSD data. The office action further asserts that the OSD memory size may be expanded or any of the other blocks expanded. Applicants respectfully disagree. Cottle et al., in column 10, lines 16-29, describe that the OSD may be stored in the SDRAM 312 or in an external memory. By default the OSD is stored in the SDRAM 312. Applications that require large quantities of OSD data preferably store them in an external memory attached to the extension bus 300. Based on a user application request, the ARM CPU 220 will turn the OSD function on and specify how and where the OSD will be mixed and displayed along with the normal video sequence. Cottle et al., however, do not indicate that the OSD data is transferred from SDRAM 312 to Data RAM 240. Cottle et al. neither disclose nor suggest that OSD data is transferred back from the Data RAM 240 to the SDRAM 312. Consequently, as previously stated, Cottle et al. neither disclose nor suggest the first memory is adapted "to transfer said on-screen display data back to the second memory in response to a request for display of data stored in the first memory" as recited in claim 1 of the present invention.

The Office Action further contends that Cottle et al. teaches that firmware is allowed access to any memory, while the OS is allowed access to most memory, and the application software is only allowed access to restricted portions of the DRAM 312 and SRAM 240, but is allowed access to all other external memory. Applicants respectfully disagree. In Cottle et al., as described in column 19, lines 26-32, a protection block implements three levels of protection for the memory space of the ARM CPU 220. Cottle et al., however, neither disclose nor suggest that the OSD requires specific allocation for specific access. In the present claimed invention, the on-screen data which is not displayed any more is transferred to a "first memory" which is used for video decompression and is transferred back to the "second memory" which is

the processor memory in response to a request to display the data. Therefore, Cottle et al. neither disclose nor suggest an OSD display circuit "wherein the first memory is adapted to receive on-screen display data that is no longer being displayed from the second memory and to transfer said on-screen display data back to the second memory in response to a request for display of data stored in the first memory" as recited in claim 1 of the present invention. Indeed any OSD data, whether stored in SDRAM 312 or an external data RAM 240, can be transferred to the OSD circuit 270, either through a DMA from SDRAM 312, or through a double DMA, first from the external memory on the extension bus to the internal data memory 240 and then to the OSD circuit 270. So, even if OSD data were transferred from the SDRAM 312 to an external memory, which is neither disclosed nor suggested by Cottle et al., there is neither any indication nor any need that, upon request for display data, data from any external memory would be transferred back to the SDRAM as in the present claimed invention.

Additionally, Cottle et al. neither disclose nor suggest "a processing unit, wherein the first memory not being directly accessible by the processing unit" as recited in claim 2 of the present invention. Specifically, as stated above regarding the rejection to claim 1, the memory units are both accessible by the processor 220 as clearly shown in Figure 1B of Cottle et al. Thus, as the processor is able to access "the first memory...and the second memory" the circuit disclosed by Cottle et al. is not equivalent to the circuit as claimed in claim 2 of the present invention, whereby the first memory is not "directly accessible by the processing unit.".

Additionally, Cottle et al. neither disclose nor suggest the "process of controlling a video apparatus comprising a digital decoder...comprising the steps of writing on-screen display data to the second memory for access by the on-screen display circuit; wherein, the first memory is used for video decompression" as recited in claim 6 of the present invention. Cottle et al. also neither disclose nor suggest "transferring on-screen display data that is no longer being be displayed to the first memory; and upon request, transferring back on-screen display data from the first memory to the second memory" as recited in claim 6 of the present invention.

The Office Action states that Cottle et al. teach data transform from/to SDRAM 312 and Data Ram 240. While any OSD data, be it stored in SDRAM 312 or an external memory, can be transferred to the OSD circuit 270 either through a DMA from SDRAM 312, or through a double DMA, first from the external memory on the extension bus to the internal data memory 240 and then to the OSD circuit 270. Cottle et al., however, neither disclose nor suggest that the OSD data transfer from SDRAM 312 to Data RAM 240 and vice versa. Column 10, lines 16-23, of Cottle et al. describes that on a request from a user, the ARM 220 will turn on the OSD function and will specify how and where the OSD will be mixed and displayed along with the normal video sequence. Cottle et al., however, neither disclose nor suggest that the OSD data is transferred from a memory to another memory before being mixed and displayed with the video sequence, as in the present claimed invention. Consequently, Cottle et al. neither disclose nor suggest "transfer[ring] said on-screen display data back to the second memory in response to a request for display of data stored in the first memory" as recited in the present claimed invention.

In view of the above remarks and amendments to the claims, it is respectfully submitted that there is no 35 USC 112 enabling disclosure provided by Cottle et al. that would make the present invention as claimed in claims 1 and 6 unpatentable. As claims 2, 4-5 and 10-11 are dependent on claim 1 and as claims 7-9 are dependent on claim 6, it is respectfully submitted that claims 2, 4-5 and 7-11 are also patentable over Cottle et al. for the reasons discussed above with respect to claims 1 and 6. Thus, it is further respectfully submitted that this rejection has been satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections, it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's attorney at the phone number below, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,
Edouard Ritz et al.

By: _____
Jack Schwartz
Reg. No. 34,721
Tel. No. (609)734-6866

Thomson Licensing Inc.
Patent Operations
PO Box 5312
Princeton, NJ 08543-5312
September 16, 2005

CERTIFICATE OF MAILING under 37 C.F.R. §1.8

I hereby certify that this amendment is being deposited with the United States Postal Service as First Class Mail, postage prepaid, in an envelope addressed to Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on:

Date: September 16, 2005

Jack Schwartz
Reg. No. 34,721